REMARKS

Claims 1-20 are pending in the application. Applicants respectfully request to cancel claim 7 without prejudice. Claims 3, 4, 5, 8, 9, 16, 17, 18 and 19 are amended. Claim 20 has been added to claim additional subject matter to which Applicants believe they are entitled. No new matter has been added.

CONCLUSION

Because no new matter has been added, Applicants respectfully submit that the above referenced patent application is entitled to the original filing date of August 28, 2001.

Please telephone the undersigned at (512) 794-3600 if there are any questions.

EXPRESS MAIL MAILING LABEL NO:

EL764881576US

Respectfully submitted,

D'Ann Naylor Rifai
Attorney for Applicant(s)
Reg. No. 47,026

Version with Markings to Show Changes Made

In the Claims

3. (Amended) The computer processor of Claim 1 wherein:

executing the instruction comprises reading a first memory location and conditionally or unconditionally writing a second memory location; and

the resource comprises the second memory location to be written.

4. (Amended) The computer processor of Claim 3 further comprising:

a cache, wherein

the cache corresponds to the resource and comprises the second memory location ~~memory location to be written is a memory location in said cache~~.

5. (Amended) The computer processor of Claim 3 wherein

the ~~circuitry~~ processor is operable to perform the reading before the processor has determined whether the instruction is to be canceled.

7. (Canceled). ~~The processor of Claim 1 wherein instruction execution is pipelined, and~~

~~if the processor determines before a pipeline stage of stages in which the unlocking is performed that the instruction is to be canceled, the instruction proceeds through all the pipeline stages at least up to, and including, the stage or stages in which the resource is unlocked.~~

8. (Amended) The processor of Claim 1 wherein:

each instruction is executed in a plurality of pipeline stages, wherein the pipeline stages for each instruction ~~includes~~ include a stage ST1 in which a signal is generated by the processor to indicate whether the instruction is to be canceled due to a trap; and

when executing the instruction which locks and then unlocks the computer resource, the processor is operable to lock the computer resource before the stage ST1.

9. (Amended) The processor of Claim 8 wherein

for at least some instructions including the instruction that locks and then ~~locks~~ unlocks the computer resource, the stage ST1 is followed by a stage ST2 in which at least one instruction result is written to an architecture storage location; and

when the processor executes the instruction that locks and then unlocks the computer resource, and the instruction is to be canceled, the stage ST2 is executed for the instruction to unlock the resource but writing to the architecture storage location is suppressed.

16. (Amended) The method of Claim 14 wherein

the instruction execution is pipelined, and

the instruction is canceled if a trap condition occurs after the ~~instructions~~ instruction processing by the processor has begun.

17. (Amended) The method of Claim 14 wherein

the instruction is an atomic instruction which comprises reading a first memory location and conditionally or unconditionally writing a second memory location; and

the resource comprises the second memory location to be written.

18. (Amended) The method of Claim 17 wherein

the second memory location to be written is a cache memory location.

19. (Amended) The method of Claim 17 wherein

the reading ~~operation~~ is performed before the processor has determined whether the instruction is to be canceled.

20. (New) The method of Claim 3 wherein

the first memory location and the second memory location correspond to the same memory location.